

1 概述

UIF2256 是一款 256 通道模拟前端 (AFE)，可满足基于平板检测器 (FPD) 的数字 X 射线成像系统的要求。采用 COF (Chip On Flex) 封装，可直接安装在数字 X 射线平板上。UIF2256 包含 256 个低功耗、低噪声、低输入电流积分器和相关双采样 (CDS) 模块；采样速度快，分辨率高。

UIF2256 具有四个 16 位分辨率 ADC，来自 ADC 的串行数据采用低压差分 (LVDS) 格式输出。控制机通过 SPI 接口对 UIF2256 进行配置。

UIF2256 支持打盹模式 (Nap Mode) 与断电模式 (Power Down)，可大幅降低功耗。

1.1 关键特性

- 256 个电荷——数字转换通道
- 16bit 分辨率，无失码
- 同步采样
- 输入范围可调，最大 9.6pC
- 扫描时间最短 12.8μs
- 超低噪声：1080e⁻ (输入 1.2 pC)
- INL: ±4 LSBs
- 每通道功耗 1.4mW (扫描时间 51.2μs)
- 休眠功耗每通道 1.12 uW

- 高密度封装，Chip On Flex
- LVDS/CMOS 串口
- 寄存器配置接口 SPI

1.2 应用领域

UIF2256 适用于多种设备:

- 数字 x 射线平板读数
- 光电二极管传感器阵列
- 多通道电荷采集系统 (电流/电压输入)

1.3 功能框图

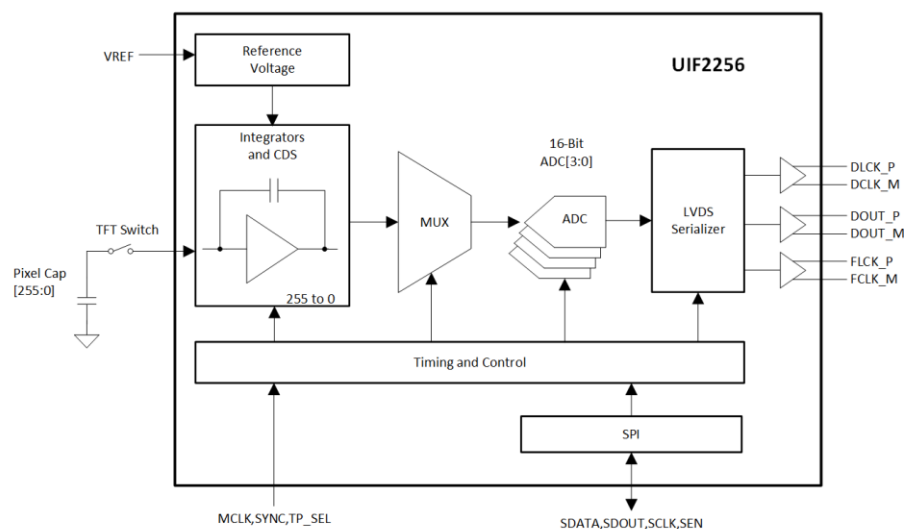


图 1-1 UIF2256 功能框图

1.4 产品型号说明

本产品提供两种封装形式：UIF2256-UYT 和 UIF2256-UYT-R。两者在封装尺寸、引脚定义及对应应用框图上存在差异，但核心功能与电气性能完全相同。

为便于不同客户场景的追溯管理，每种封装分别提供带标识后缀“D”的丝印版本，形成表 1-1 所列四款丝印型号。

表 1-1 UIF2256 丝印型号

封装形式	标准丝印	D 版丝印
封装 1 (UYT)	UIF2256-UYT	UIF2256D-UYT
封装 2 (UYT-R)	UIF2256-UYT-R	UIF2256D-UYT-R

注：同一行内两款丝印型号的封装、引脚、性能、规格及功能完全一致，仅丝印字符存在差异。

本文档型号约定如下：

- 统称：如无特殊说明，文中“UIF2256”统称上述所有丝印型号，其描述内容适用于四款产品。
- 区分：当需要区分封装时，型号对应关系如下：
 - ◆ UIF2256-UYT ——涵盖 UIF2256-UYT 及 UIF2256D-UYT；
 - ◆ UIF2256-UYT-R ——涵盖 UIF2256-UYT-R 及 UIF2256D-UYT-R。

2 引脚定义与功能

2.1 UIF2256-UYT

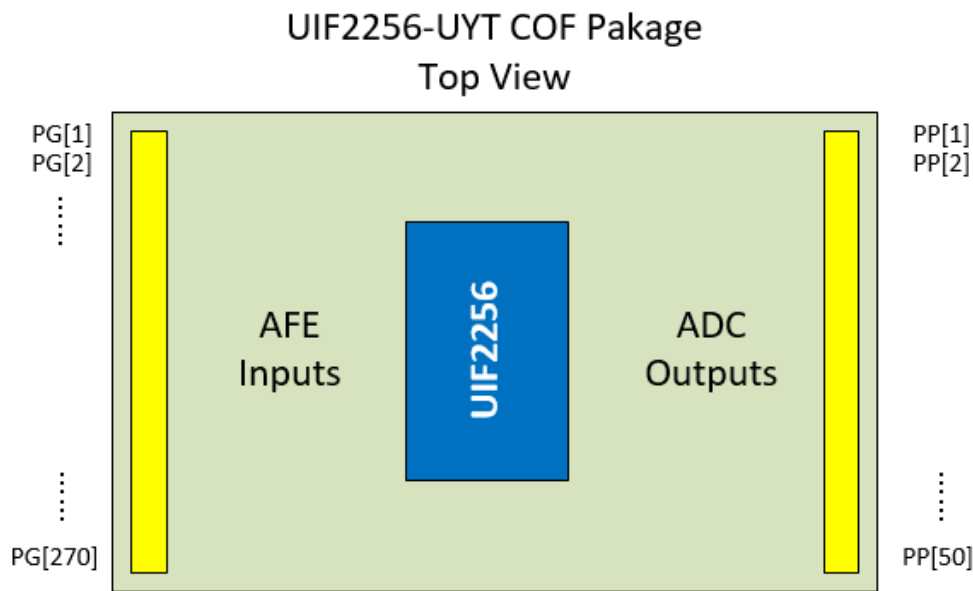


图 2-1 UIF2256-UYT 引脚图

表 2-1 UIF2256-UYT 引脚定义：连玻璃端

COF Pad		No. of Pads	I/O	Description	Glass Connection
No.	Name				
PG[1:3]	FLOAT	3	I/O	Not connected	N/A
PG[4:6]	VBIAS	3	I/O	Pass-through connection to PP[1]	Photodiode bias
PG[7]	VB	1	O	Pass-through connection to PP[2] as shield trace	Float and route adjacent to IN[255] as a shield
PG[8:263]	IN[0:255]	256	I	Analog input channels	From FPD sensor
PG[264]	VB	1	O	Pass-through connection to PP[49] as shield trace	Float and route adjacent to IN[0] as a shield
PG[265:267]	VBIAS	3	I/O	Pass-through connection to PP[50]	Photodiode bias
PG[268:270]	FLOAT	3	I/O	Not connected	N/A

A = analog, D = digital, I = input, N/A = not applicable, O = output

表 2-2 UIF2256-UYT 引脚定义：连 PCB 端

COF Pad		I/O	Analog or Digital	Description	PCB Connection
No.	Name				
PP[1]	VBIAS	I/O	Analog	Photodiode bias; pass-through connection to PG[4:6]	Low-noise voltage source
PP[2]	EXTC_I	I	Analog	Input reference for integrator positive terminal	22 μ F+1 μ F+0.1 μ F capacitor (preferably X5R-type) to ground plane.
PP[3]	AVSS	I	Analog	Analog ground	Ground plane
PP[4]	AVSS	I	Analog	Analog ground	Ground plane
PP[5]	AVDD1	I	Analog	Analog supply	1.8 V
PP[6]	AVDD2	I	Analog	Analog supply	3.3 V
PP[7]	AVSS	I	Analog	Analog ground	Ground plane
PP[8]	AVSS	I	Analog	Analog ground	Ground plane
PP[9]	AVSS	I	Analog	Analog ground	Ground plane
PP[10]	AVDD1	I	Analog	Analog supply	1.8 V
PP[11]	AVSS	I	Analog	Analog ground	Ground plane
PP[12]	AVDD1	I	Analog	Analog supply	1.8 V
PP[13]	AVSS	I	Analog	Analog ground	Ground plane
PP[14]	DOUTP	O	Digital	Low-voltage differential signaling (LVDS) data output	To field-programmable gate array (FPGA)
PP[15]	DOUTM	O	Digital	LVDS data output	To FPGA
PP[16]	FCLKP	O	Digital	LVDS frame clock	To FPGA
PP[17]	FCLKM	O	Digital	LVDS frame clock	To FPGA
PP[18]	DCLKP	O	Digital	LVDS data clock	To FPGA
PP[19]	DCLKM	O	Digital	LVDS data clock	To FPGA
PP[20]	AVSS	I	Analog	Analog ground	Ground plane
PP[21]	AVDD1	I	Analog	Analog supply	1.8 V
PP[22]	AVDD1	I	Analog	Analog supply	1.8 V
PP[23]	MCLK	I	Digital	Master clock input(10M~20M)	From FPGA
PP[24]	SYNC	I	Digital	Synchronization pulse input	From FPGA
PP[25]	TP_SEL	I	Digital	Timing profile selection	From FPGA
PP[26]	SDOUT	O	Digital	Serial interface data output	To FPGA
PP[27]	SCLK	I	Digital	Serial interface clock input	From FPGA
PP[28]	SDATA	I	Digital	Serial interface data input	From FPGA
PP[29]	SEN	I	Digital	Serial interface enable	From FPGA
PP[30]	COMP4	I	Analog	Analog input for TFT charge compensation	Output of low-noise digital-to-analog converters (DACs). These pins can be connected to the ground plane if not used.
PP[31]	COMP3	I	Analog		
PP[32]	COMP2	I	Analog		
PP[33]	COMP1	I	Analog		
PP[34]	AVSS	I	Analog	Analog ground	Ground plane
PP[35]	AVDD1	I	Analog	Analog supply	1.8 V
PP[36]	AVSS	I	Analog	Analog ground	Ground plane

COF Pad		I/O	Analog or Digital	Description	PCB Connection
No.	Name				
PP[37]	AVDD1	I	Analog	Analog supply	1.8 V
PP[38]	AVSS	I	Analog	Analog ground	Ground plane
PP[39]	AVDD1	I	Analog	Analog supply	1.8 V
PP[40]	AVSSC	I	Analog	Analog ground	Ground plane
PP[41]	VREF	I	Analog	Reference voltage	Low-noise 1.25V reference
PP[42]	EXTC_O	I/O	Analog	Not connected	N/A
PP[43]	VTESTC	O	Analog	Probe pad	Test point
PP[44]	AVSS	I	Analog	Analog ground	Ground plane
PP[45]	AVDD2	I	Analog	Analog supply	3.3 V
PP[46]	AVDD1	I	Analog	Analog supply	1.8 V
PP[47]	AVSS	I	Analog	Analog ground	Ground plane
PP[48]	AVSS	I	Analog	Analog ground	Ground plane
PP[49]	EXTC_I	I	Analog	Input reference for integrator positive terminal	This pin requires an externally supplied voltage of 0.95 V (can be derived from VREF via voltage division) and 22μF+1μF+0.1μF capacitor (preferably X5R-type) to ground plane.
PP[50]	VBIAS	I/O	Analog	Photodiode bias; pass-through connection to PG[265:267]	Low-noise voltage source

A = analog, D = digital, I = input, N/A = no applicable, O = output

2.2 UIF2256-UYT-R

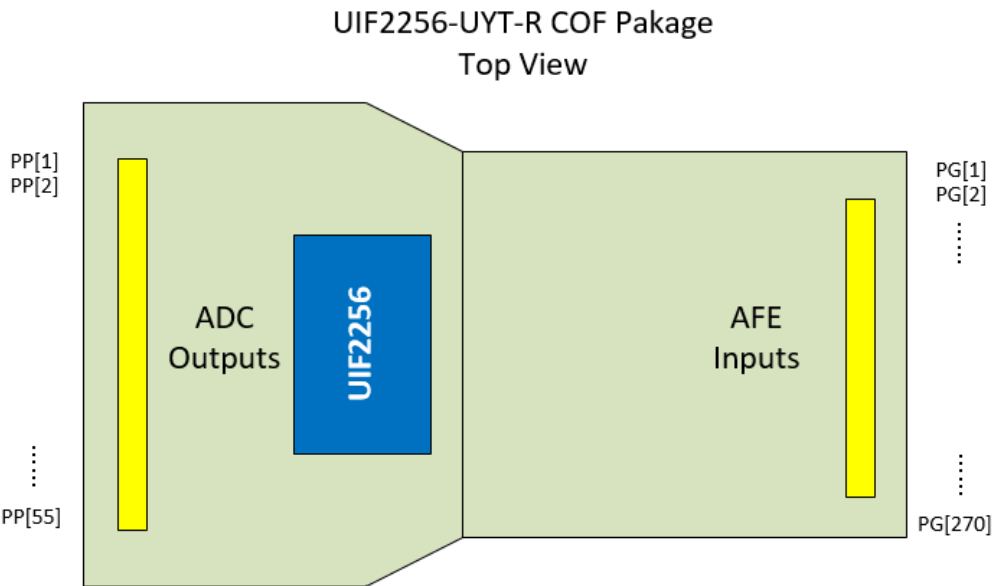


图 2-2 UIF2256-UYT-R 引脚图

表 2-3 UIF2256-UYT-R 引脚定义：连玻璃端

COF Pad		No. of Pads	I/O	Description	Glass Connection
No.	Name				
PG[1:4]	PASSTHROU 1	4	I/O	Passthrough connection to PP[1:2]	Reserved
PG[5:6]	PASSTHROU 2	2	I/O	Passthrough connection to PP[3:4]	Reserved
PG[7]	VB	1	O	Shield voltage biased at EXTC_I voltage	Float and route adjacent to IN[255] as a shield
PG[8:263]	IN[0:255]	256	I	Analog input channels	From FPD sensor
PG[264]	VB	1	O	Shield voltage biased at EXTC_I voltage	Float and route adjacent to IN[255] as a shield
PG[265:266]	PASSTHROU 3	2	I/O	Passthrough connection to PP[53]	Reserved
PG[267:270]	PASSTHROU 4	4	I/O	Passthrough connection to PP[54:55]	Reserved

A = analog, D = digital, I = input, N/A = not applicable, O = output

表 2-4 UIF2256-UYT-R 引脚定义：连 PCB 端

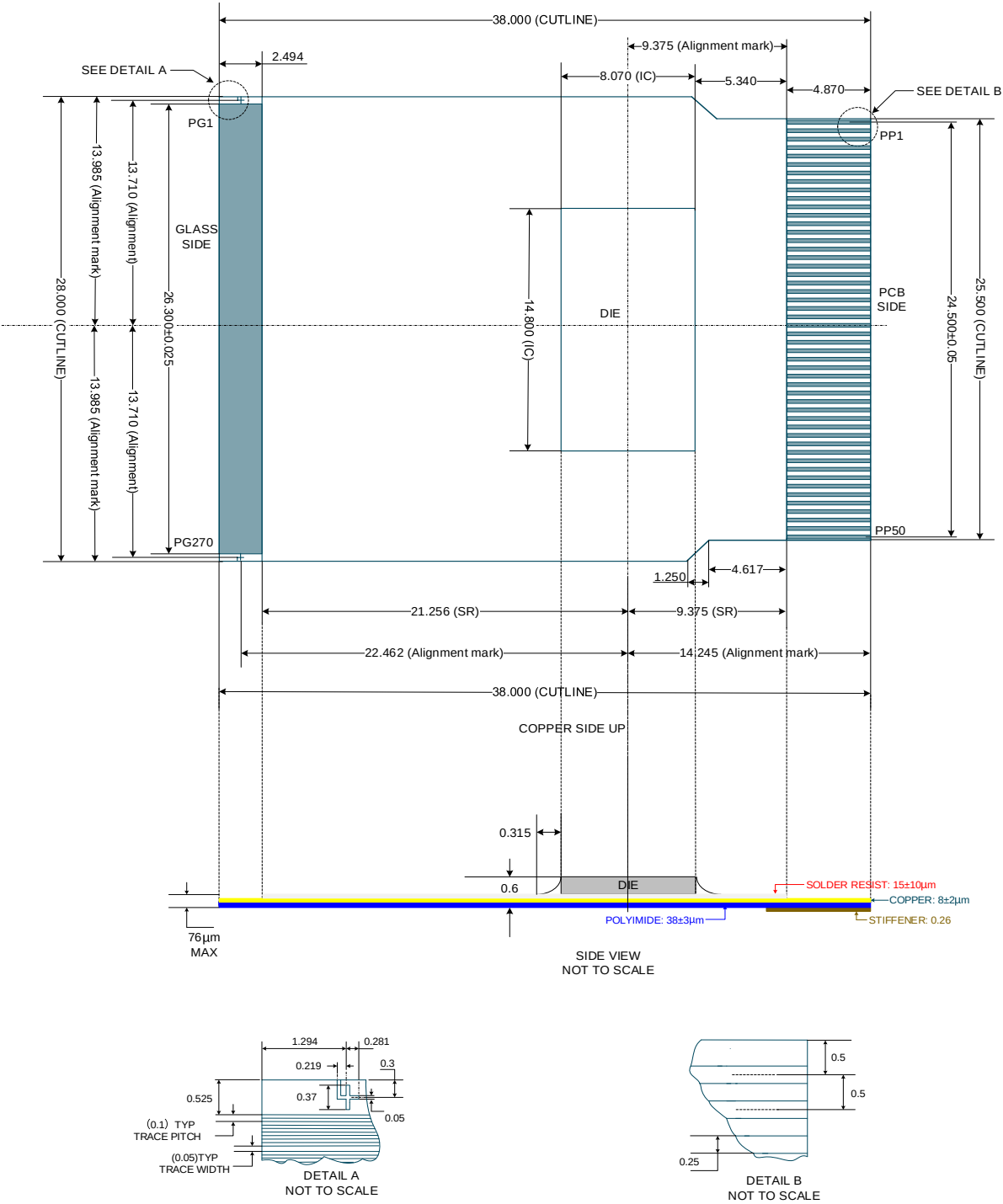
COF Pad		I/O	Analog or Digital	Description	PCB Connection
No.	Name				
PP[1:2]	PASSTHROU1	I/O	Analog	Passthrough connection to PG[1:4]	Reserved
PP[3:4]	PASSTHROU2	I/O	Analog	Passthrough connection to PG[5:6]	Reserved
PP[5]	EXTC_I	I	Analog	Input reference for integrator positive terminal	22μF+1μF+0.1μF capacitor (preferably X5R-type) to ground plane.
PP[6]	AVSS	I	Analog	Analog ground	Ground plane
PP[7]	AVSS	I	Analog	Analog ground	Ground plane
PP[8]	AVDD1	I	Analog	Analog supply	1.8 V
PP[9]	AVDD2	I	Analog	Analog supply	3.3 V
PP[10]	AVSS	I	Analog	Analog ground	Ground plane
PP[11]	AVSS	I	Analog	Analog ground	Ground plane
PP[12]	AVSS	I	Analog	Analog ground	Ground plane
PP[13]	AVDD1	I	Analog	Analog supply	1.8 V
PP[14]	AVSS	I	Analog	Analog ground	Ground plane
PP[15]	AVDD1	I	Analog	Analog supply	1.8 V
PP[16]	AVSS	I	Analog	Analog ground	Ground plane
PP[17]	DOUTP	O	Digital	Low-voltage differential signaling (LVDS) data output	To field-programmable gate array (FPGA)
PP[18]	DOUTM	O	Digital	LVDS data output	To FPGA
PP[19]	FCLKP	O	Digital	LVDS frame clock	To FPGA
PP[20]	FCLKM	O	Digital	LVDS frame clock	To FPGA
PP[21]	DCLKP	O	Digital	LVDS data clock	To FPGA

COF Pad		I/O	Analog or Digital	Description	PCB Connection
No.	Name				
PP[22]	DCLKM	O	Digital	LVDS data clock	To FPGA
PP[23]	AVSS	I	Analog	Analog ground	Ground plane
PP[24]	AVDD1	I	Analog	Analog supply	1.8 V
PP[25]	AVDD1	I	Analog	Analog supply	1.8 V
PP[26]	MCLK	I	Digital	Master clock input(10M~20M)	From FPGA
PP[27]	SYNC	I	Digital	Synchronization pulse input	From FPGA
PP[28]	TP_SEL	I	Digital	Timing profile selection	From FPGA
PP[29]	SDOUT	O	Digital	Serial interface data output	To FPGA
PP[30]	SCLK	I	Digital	Serial interface clock input	From FPGA
PP[31]	SDATA	I	Digital	Serial interface data input	From FPGA
PP[32]	SEN	I	Digital	Serial interface enable	From FPGA
PP[33]	COMP4	I	Analog	Analog input for TFT charge compensation	Output of low-noise digital-to-analog converters (DACs). These pins can be connected to the ground plane if not used.
PP[34]	COMP3	I	Analog		
PP[35]	COMP2	I	Analog		
PP[36]	COMP1	I	Analog		
PP[37]	AVSS	I	Analog	Analog ground	Ground plane
PP[38]	AVDD1	I	Analog	Analog supply	1.8 V
PP[39]	AVSS	I	Analog	Analog ground	Ground plane
PP[40]	AVDD1	I	Analog	Analog supply	1.8 V
PP[41]	AVSS	I	Analog	Analog ground	Ground plane
PP[42]	AVDD1	I	Analog	Analog supply	1.8 V
PP[43]	AVSS	I	Analog	Analog ground	Ground plane
PP[44]	VREF	I	Analog	Reference voltage	Low-noise 1.25V reference
PP[45]	EXTC_O	I/O	Analog	Not connected	N/A
PP[46]	VTESTC	O	Analog	Probe pad	Test point
PP[47]	AVSS	I	Analog	Analog ground	Ground plane
PP[48]	AVDD2	I	Analog	Analog supply	3.3 V
PP[49]	AVDD1	I	Analog	Analog supply	1.8 V
PP[50]	AVSS	I	Analog	Analog ground	Ground plane
PP[51]	AVSS	I	Analog	Analog ground	Ground plane
PP[52]	EXTC_I	I	Analog	Input reference for integrator positive terminal	This pin requires an externally supplied voltage of 0.95 V (can be derived from VREF via voltage division) and 22μF+1μF+0.1μF capacitor (preferably X5R-type) to ground plane.
PP[53]	PASSTHROU3	I/O	Analog	Passthrough connection to PG[265:266]	Reserved
PP[54:55]	PASSTHROU4	I/O	Analog	Passthrough connection to PG[267:270]	Reserved

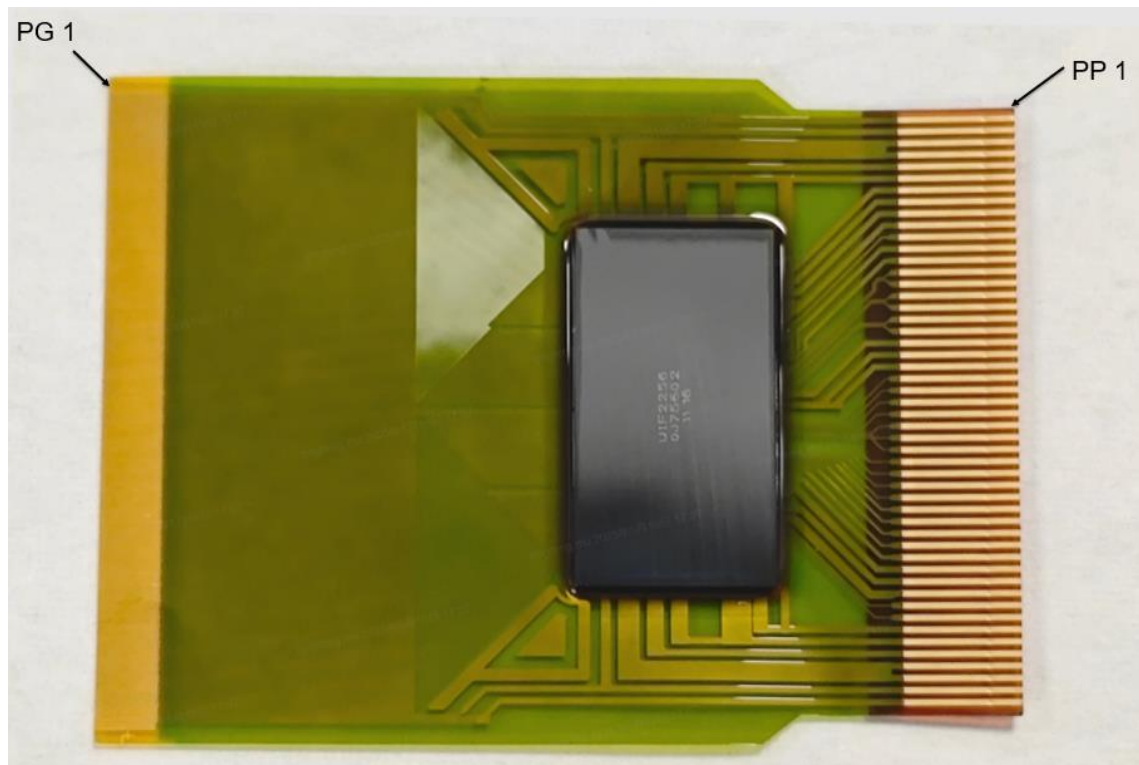
A = analog, D = digital, I = input, N/A = no applicable, O = output

3 封装尺寸

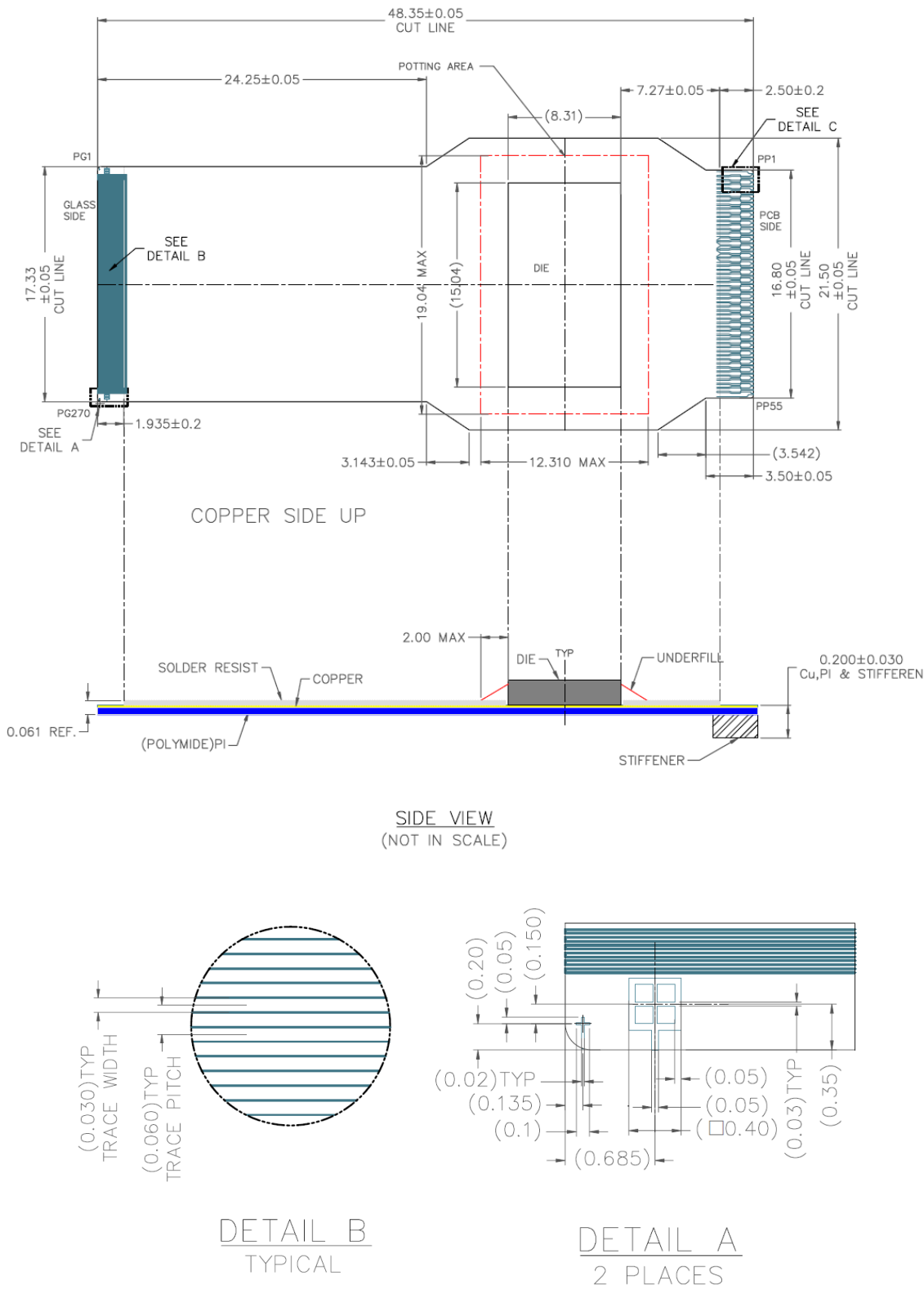
3.1 UIF2256-UYT 封装示意图及实物图

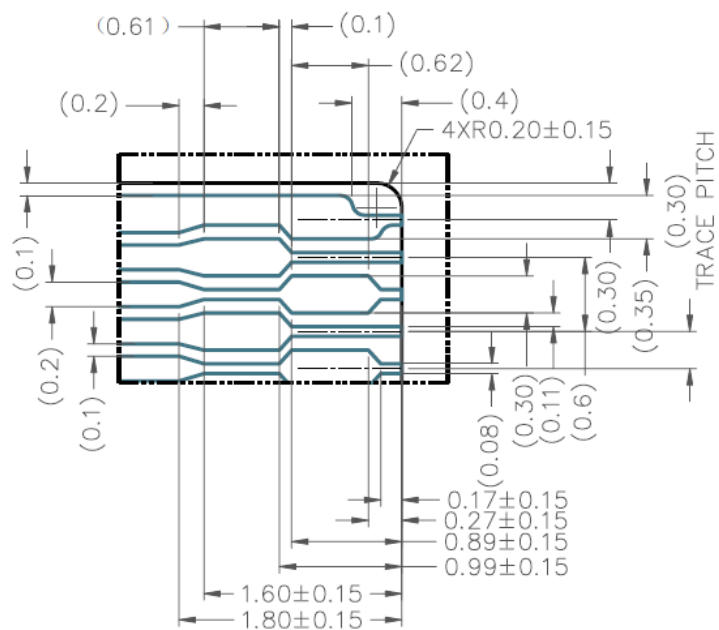


Interface Stack Structure	Thickness (mm)
Stiffener	0.26
PI	0.038
Cu	0.008
Solder Resist	0.015



3.2 UIF2256-UYT-R 的封装示意图及实物图





DETAIL C

Interface Stack Structure	Thickness (mm)
Stiffener+Cu+PI	0.2±0.03

